UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,922,367 B2

APPLICATION NO.: 10/617246 DATED: July 26, 2005

INVENTOR(S) : Christopher K. Morzano and Wen Li

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Item (57), Line 3 Column 1, Line 51 Column 2, Line 31 Column 3, Lines 31 and 32	"respective enable signal" "conventional DDR memory device," "diagram a data strobe" "complimentary"	a respective enable signalconventional DDR memory devices,diagram of a data strobecomplementary
Column 3, Line 57 Column 3, Lines 65-67	"compliment" "Returning to FIG. 1, since the logic circuits 46, 48, the ENA and ENB signals that enable the logic circuits 46, 48 are generated by a flip-flop."	complementReturning to FIG. 1, since the ENA and ENB signals that enable the logic circuits 46, 48 are generated by a flip-flop 60, they are enabled at the same time,
Column 5, Line 62 Column 6, Line 9	"through the nor gate" "and RAMBUS DRAMs (RDRAMS"),"	through the NOR gate and RAMBUS DRAMs ("RDRAMS"),
Colum 6, Line 18	"memory arrays 120, 12"	memory arrays 120, 122
Column 7, Line 5	"which the"	with the
Column 8, Line 9	"applied to control input"	applied to a control input
Column 8, Line 13	"being compliments"	being complements
Column 8, Lines 14-15	"logic circuit in enabled"	logic circuit is enabled
Column 8, Line 30	"coupled to reset"	coupled to the reset
Column 9, Line 23	"applied to an control input"	applied to a control input
Column 9, Line 27	"compliments"	complements
Column 9, Lines 28-29	"logic circuit in enabled"	logic circuit is enabled
Column 9, Lines 43-44	"coupled to reset input"	coupled to the reset input
Column 10, Line 33	"coupled the external data terminal"	coupled to the external data terminal
Column 10, Line 40	"applied to an control input"	applied to a control input
Column 10, Line 44	"being compliments"	being complements
Column 10, Lines 45-46	"second logic circuit in enable"	second logic circuit is enabled

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Column, Line	Reads	Should Read
Column 10, Line 61	"coupled to reset"	coupled to the reset
Column 12, Line 12	"applied to an control input"	applied to a control input
Column 12, Line 16	"compliments"	complements
Column 12, Lines 17-18	"logic circuit in enabled"	logic circuit is enabled
Column 13, Lines 28-29	"being operable to	being operable to make
	generate make the first enable signal"	the first enable signal
Column 13, Line 43	"applied to an control input"	applied to a control input
Column 13, Line 47	"compliments"	complements
Column 13, Line 48-49	"logic circuit in enabled"	logic circuit is enabled
Column 13, Line 63	"circuit farther"	circuit further
Column 15, Line 28	"applied to an control input"	applied to a control input
Column 15, Line 32	"compliments"	complements
Column 15, Lines 33-34	"logic circuit in enabled"	logic circuit is enabled
Column 16, Lines 5 and 17	"the method comprises:"	the method comprising:

Signed and Sealed this

Twenty-fifth Day of December, 2007

JON W. DUDAS
Director of the United States Patent and Trademark Office